WE CLAIM:

1. A surface-mount semiconductor device package comprising:

a substrate having at least one planar surface;

a semiconductor device disposed on the planar surface of the substrate; and

an encapsulant surrounding the semiconductor device wherein the encapsulant material has thermal expansion properties substantially similar to the thermal expansion properties of the substrate.

2. A surface-mount semiconductor device package according to claim 1 wherein the package thermal resistance is less than about 200 degrees Centigrade per Watt.

3. A surface-mount semiconductor device package according to claim 1 wherein the package thermal resistance is less than about 50 degrees Centigrade per Watt.

4. A surface-mount semiconductor device package according to claim 1 wherein the package thermal resistance is less than approximately 25 degrees Centigrade per Watt.

5 3. A surface-mount semiconductor device package according to claim 1 further comprising a plurality of conductive pads disposed on a surface of the substrate and electrically bonded to the semiconductor device.

4. A surface-mount semiconductor device package according to claim 3 further comprising conductive leads for electrically coupling the conductive pads to the semiconductor device.

5. A surface-mount semiconductor device package according to claim 1 wherein the substrate comprises ceramic material.

6. A surface-mount semiconductor device package according to claim 1 wherein the substrate comprises alumina.

7. A surface-mount semiconductor device package according to claim 1 wherein the substrate comprises beryllia.

8. A surface-mount semiconductor device package according to claim 1 wherein the encapsulant material comprises epoxy resin.

9. A surface-mount semiconductor device package according to claim 1 wherein the encapsulant material comprises Dexter FP4451 epoxy resin.

10. A surface-mount semiconductor device package according to claim 1 wherein the semiconductor device is operable at frequencies within a range of about 2-10 GHz.

11. A surface-mount semiconductor device package according to claim 1 wherein the semiconductor device is operable at frequencies within a range of about 10-12 GHz.

14 ~~12~~. A surface-mount semiconductor device package comprising:

a planar ceramic substrate having a first surface and an opposing second surface;

a semiconductor device disposed on the substrate first surface;

conductive pads disposed on the substrate second surface;

conductive leads coupling the semiconductor device to the conductive pads; and

a low dielectric constant encapsulant material encapsulating the semiconductor device and substrate first surface.

15 ~~13~~. A surface-mount semiconductor device package according to claim ~~12~~ 14 wherein the substrate comprises alumina.

16 ~~14~~. A surface-mount semiconductor device package according to claim ~~12~~ 14 wherein the substrate comprises beryllia.

17 ~~15~~. A surface-mount semiconductor device package according to claim ~~12~~ 14 wherein the encapsulant material comprises epoxy resin.

18 ~~16~~. A surface-mount semiconductor device package according to claim ~~12~~ 14 wherein the encapsulant material comprises Dexter FP4451 epoxy resin.

19 ~~17~~. A surface-mount semiconductor device package according to claim ~~12~~ 14 wherein the semiconductor device is operable at frequencies within a range of about 2-10 GHz.

20 ~~18~~. A surface-mount semiconductor device package according to claim ~~12~~ 14 wherein the semiconductor device is operable at frequencies within a range of about 10-12 GHz.

21 ~~19~~. A method of manufacturing a surface-mount semiconductor device package comprising:

affixing a semiconductor device to a first surface of a ceramic substrate;

affixing conductive pads to an opposing second substrate surface;

coupling the semiconductor device to the conductive pads with conductive leads; and

encapsulating the semiconductor device in a low dielectric constant encapsulant material.

22 ~~20~~. A method of manufacturing a surface-mount semiconductor device package according to claim ~~19~~ 21 wherein the step of coupling the semiconductor device to the conductive pads further comprises the step of selecting the length of the conductive leads such that the series inductance of the device package is minimized.

23 ~~21~~. A method of manufacturing a surface-mount semiconductor device package according to claim ~~19~~ 21 wherein the step of encapsulating the semiconductor device further comprises the step of selecting an encapsulant material such that the parasitic capacitance of the device package is minimized.